TEA 1007/TEA 1007-FP

Phase control circuit

General Triac Control

Technology: Bipolar

Features

- Current consumption ≤ 2.5 mA
- Ignition pulse typ. 150 mA
- Voltage and current synchronization
- Internal supply voltage control

Case: DIP 8, SO 8

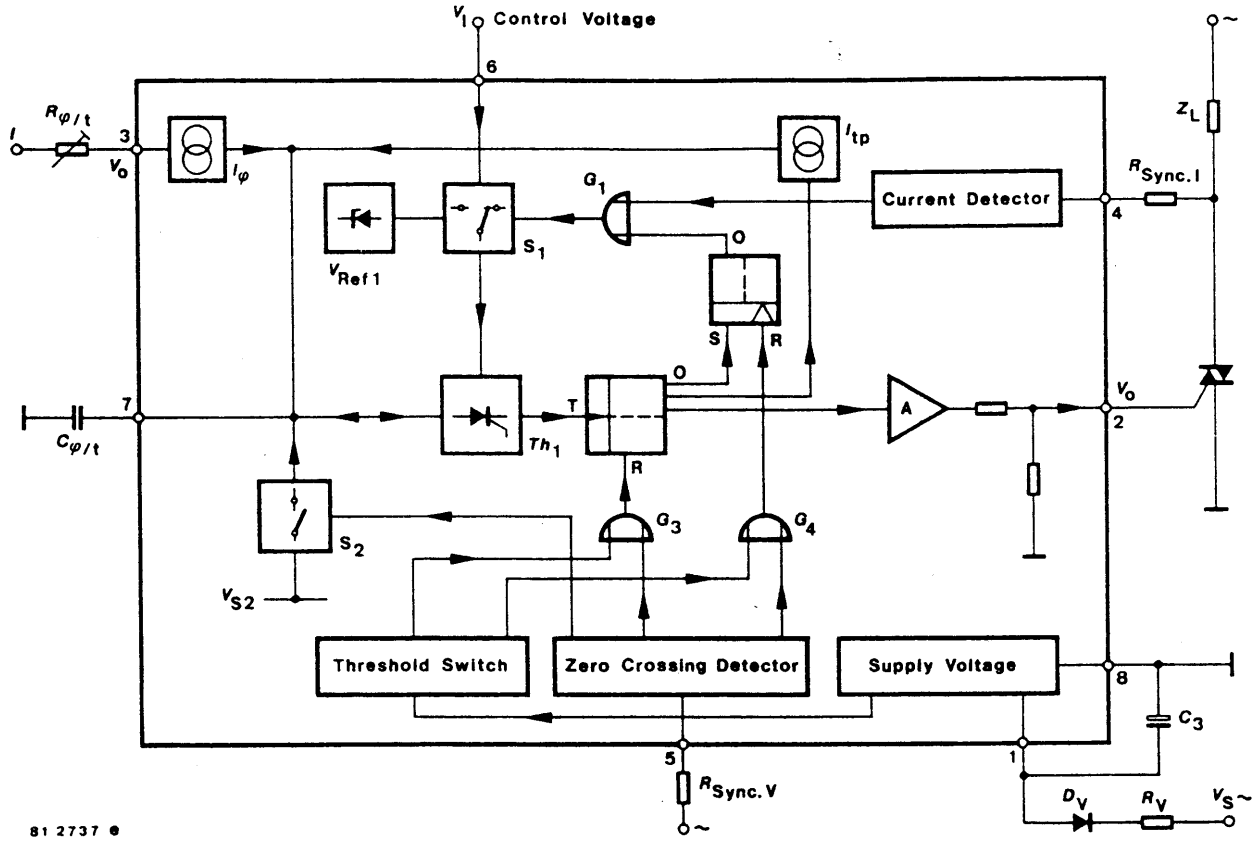


Figure 1 Block diagram with typical circuitry

Description

The phase-shift of the ignition point is determined in the usual manner by comparison between a mains synchronized ramp voltage and a predetermined required value. The capacitor $C_{\varphi/t}$ between Pin 7 and the common reference point Pin 8 is discharged at the zero transition of the mains voltage via the V_o detector, gate G_2 and switch S_2. After the end of the zero transition pulse, $C_{\varphi/t}$ is charged from the constant current source I_φ, whose value is adjusted externally with Rφ at Pin 3 due to the unavoidable tolerance of $C_{\varphi/t}$ (Phase 1).

When the potential at Pin 7 reaches the nominal value predetermined at Pin 6, the thyristor Th_1, which also functions as a comparator, ignites and sets the following clock flip-flop. The output of the clock flip-flop releases the output amplifier, connects a second constant current source to the capacitor $C_{\varphi/t}$, and switches the reference voltage switch S_1 to an internally generated threshold voltage V_{Ref1} via an RS flip-flop and the OR gate G_1.

The capacitor $C_{\varphi/t}$ is charged in this second phase by $I_\varphi + I_{tp}$ until it reaches the internal reference voltage V_{Ref}. The length of this Phase 2 corresponds to the width of the output pulse tp. When the capacitor voltage reaches the value V_{Ref}, thyristor Th_1 ignites again and resets the clock flip-flop to its initial state. The output pulse is thus terminated and the constant source I_{tp} is switched off. However, the RS flip-flop holds the switch S_1 so that the internal reference voltage remains connected to Th_1. As V_{Ref} is greater than the maximum permissible control voltage at Pin 6, this prevents more than one ignition pulse from being generated in each half-cycle of the mains voltage. This is particularly important because the energy contents of the output pulse is of the same order as the internal requirements of the circuit for each half-wave.

In the following zero transition of the mains voltage, the zero transition detector (Input Pin 5) resets the RS flip–flop, discharges $C_{\varphi/t}$ again via S_2, and also insures that the clock flip-flop is in the reset condition. A further part of the basic function is the current detector with its input at Pin 4. When controlling inductive loads, the load current lags behind the mains voltage which means that the circuit could generate an ignition pulse during the period in which currents is still flowing with a polarity opposite to that of the mains voltage if the current were not taken into account. This, in turn, would lead, to so-called ”gaps” in the load current as the next ignition pulse is generated in the subsequent half-cycle.

In indication as to whether load current is flowing or not is provided by the triac itself. When the triac is ignited, the voltage at electrode H_1 drops from the instantaneous value of the mains voltage to approx. 1.5 V, the value of the forward voltage of the triac. When the load current drops below the hold current of the triac towards the end of the half-cycle, V_{H1} again returns to the instantaneous value of the mains voltage. The current detector with its input at Pin 4 now controls this triac voltage and blocks the pulse generator via G_1 and S_1 by increasing the reference voltage as long as the triac is conducting. As, in the case of a resistive load, the triac may be extinguished shortly before the zero transition of the mains voltage – when the load current drops below the hold current – the RS flip-flop must prevent any possible second ignition pulse from being generated.

Additional function

An internal supply voltage control circuit insures that output pulses can be generated only when the supply voltage required for operation of all logic functions is available.

Series resistance R_1 can be calculated approx. as follows:

$$R_{1max} = 0.85 \ \frac{V_{Mmin} - V_{Smax}}{2 \cdot I_{tot}}$$

$I_{tot} = I_S + T_P + I_x$ whereas

I_{tot} = Total current consumption

I_S = Current requirement of the lC

I_P = Average current requirement of the triggering pulses

I_x = Current requirement of other peripheral components

Appendix gives further informations regarding the design.

Determination of gate series resistance, firing current and pulse width

Firing current requirement depends upon the triac used which can be regulated with series resistance as given below:

$$R_{G\,max} \approx \frac{12.5\ V - V_{G\,max}}{I_{G\,max}} - 110\ \Omega$$

$$I_p = \frac{I_G}{T} \times t_p$$

$$t_p \approx \frac{8\ \mu s}{nF} \times C_\varphi$$

whereas:

V_G = Triac’s gate voltage
I_G = Triac’s gate current
I_P = Gate current requirement – average
T = Mains frequency
t_p = (firing) pulse width
C_φ = Ramp capacitor

Absolute Maximum Ratings

Reference point Pin 8

Parameters		Symbol	Value	Unit
Current consumption	Pin 1	$-I_S$	30	mA
Peak current consumption t<10 µS	 Pin 1	 $-i_s$	60	mA
Sync. currents t<10 µS 	Pin 4 Pin 5 Pin 4 Pin 5	I_{syncI} I_{syncV} $\pm i_{sync.I}$ $\pm i_{sync.V}$	10 10 60 60	mA mA mA mA
Input current	Pin 3	$-I_I$	5	mA
Input voltage	Pin 6 Pin 2	$-V_I$ V_I	$\leqq V_S$ $-V_S \leqq V_I \leqq 2$	 V
Power dissipation T_{amb} = 45 °C T_{amb} = 80 °C	 	 P_{tot} P_{tot}	 400 225	 mW mW
Junction temperature		T_j	125	°C
Ambient temperature range		T_{amb}	0...80	°C
Storage temperature range		T_{stg}	–40...+125	°C
Maximum thermal resistance				
Junction ambient	DIP 8 SO 8 (P.C.) SO 8 (ceramic)	R_{thJA} R_{thJA} R_{thJA}	200 220 140	K/W K/W K/W

Electrical Characteristics

Reference point Pin 8, unless otherwise specified

Parameters	Test Conditions / Pin		Symbol	Min	Type	Max	Unit
Mains supply			$-V_S$	13.5		17	V
Current consumption			I_S			2.5	mA
Sync. currents		Pin 4 Pin 5	$I_{syncI.}$ I_{syncV}		0.35 0.65		mA mA
Output pulse current	V_S = 13.5 V, R_G = 0 V, V_G = 1.2 V	Pin 2	I_O	90		180	mA
Output pulse width	$C_{\varphi/t}$ = 3.3 nF $C_{\varphi/t}$ = 6.8 nF	Pin 2	t_p t_p	8 15		30 64	µs µs
Charge current "Phase 1"	$C_{\varphi/t}$ = 3.3 nF $C_{\varphi/t}$ = 6.8 nF	Pin 7 Pin 7 Pin 7	I_φ I_φ I_φ	1	 2 4.3	20	µA µA µA
Charge current "Phase 2"		Pin 7	I_t		1.3		mA
Drive current		Pin 6	I_i			0.5	µA
Balance between two half cycles when V_6 = constant			$\Delta\varphi$			± 3°	

Applications

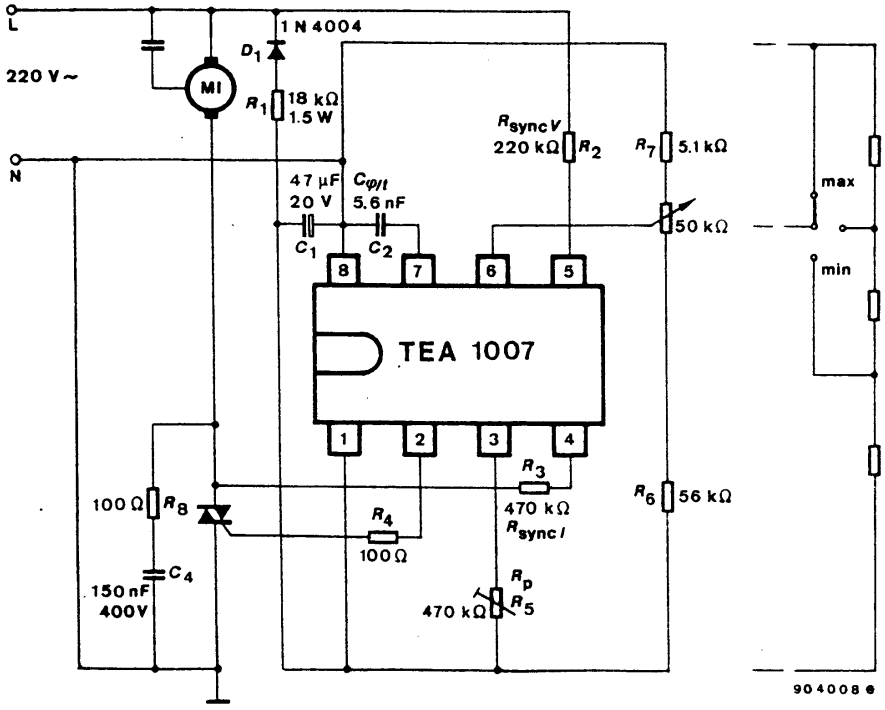


Fig. 2 Phase control for fan motors – 220 V_{ac}

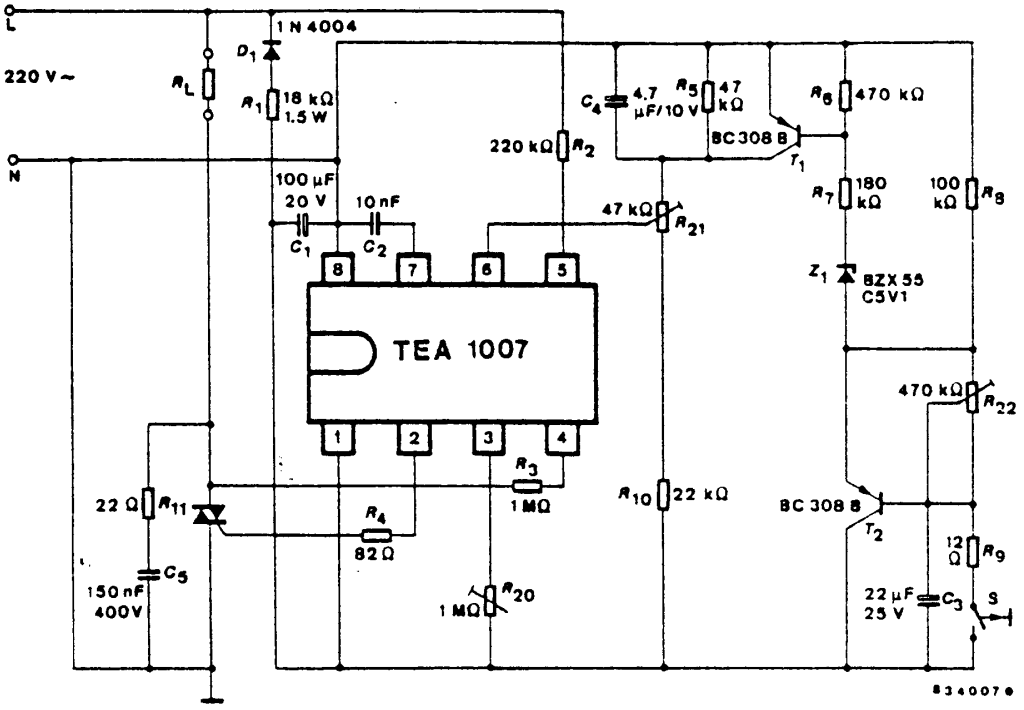


Fig. 3 Two-phase time-switch

The timing switch using the TEA 1007 permits two-phase operation of loads with conduction angle φ adjustable as required (Fig. 3).

Phase 1:	$\varphi = \varphi_{max}$	adjustable with R_{21}
	Period t = 5 ÷ 320 sec	adjustable with R_{22}
Phase 2:	$\varphi = \varphi_{min}$	adjustable with R_{20}
	Period t = optional, or up to the pressed time of switch S	

Phase 1 begins as soon as the mains voltage is applied. The maximum angle of conduction φ_{max} can be adjusted by means of R_{21}. The timing circuit comprises T_1, T_2, Z_1, C_3 and R_{22}. As the voltage to which C_3 is charged increases, the current through Z_1 decreases. When the potential at the emitter of T_2 has climbed so high that the current through Z_1 becomes zero, T_1 can no longer conduct. The potential on R_{21} therefore drops. The conduction angle φ decreases to the value φ_{min}, adjustable by means of R_{20} (Phase 2).

The transition from φ_{max} to φ_{min} takes place continuously following the adjustment of R_{22} and takes ca. 2 ... 20 secs. The time constant of Phase 1**,** which is also determined by R_{22}, begins with the release of key S. If S is pressed again before the end of the time constant, a period equal to the complete time-constant is added to the time already run.

The circuit is powered direct from mains via D_1 and R_1 in every negative half-cycle. C_1 smooths the operating voltage which settles at a level of ca. 15.5 V.

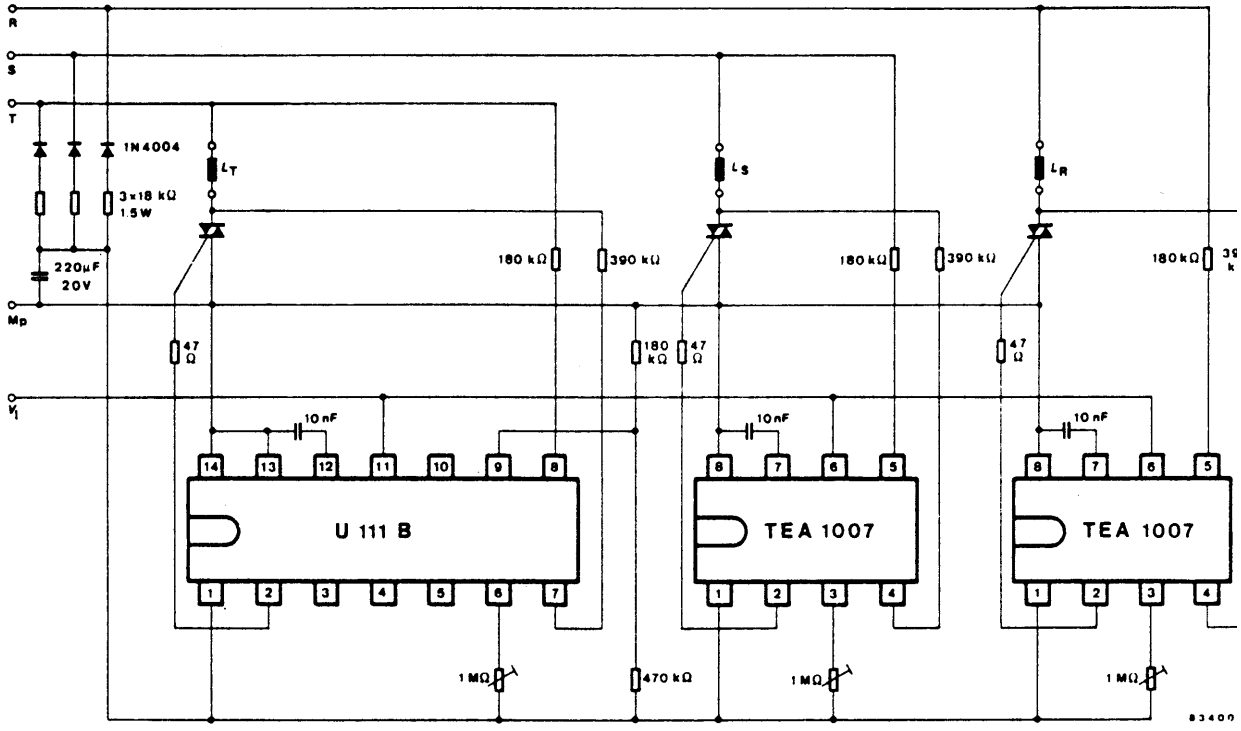


Fig. 4 Three-phase power control with U 111 B and TEA 1007

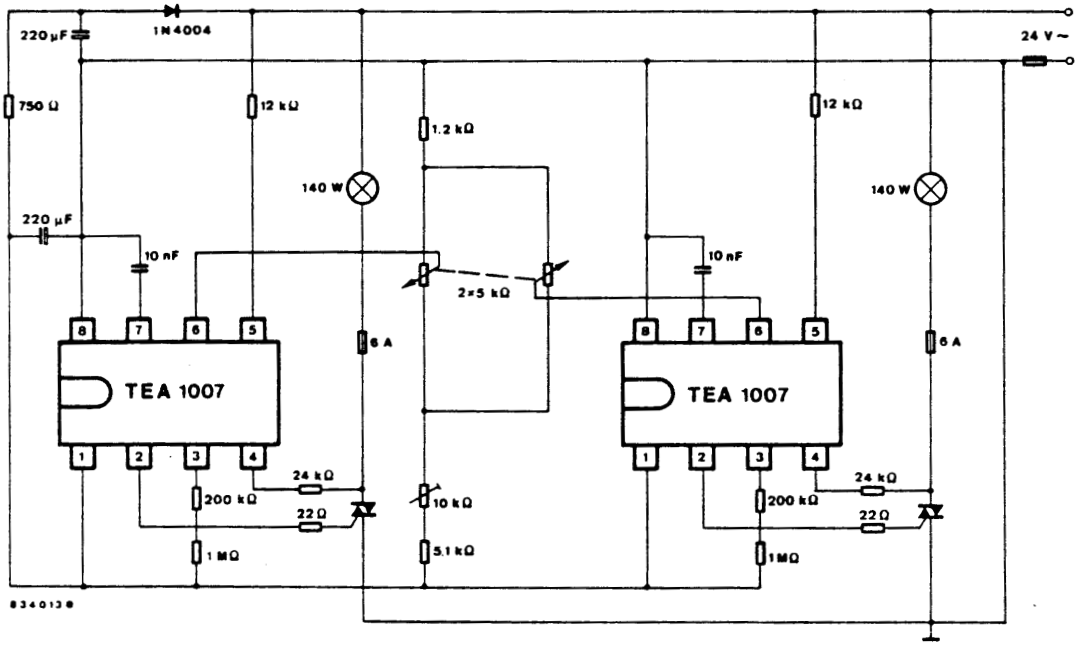


Fig. 5 Fading circuit for manual operation

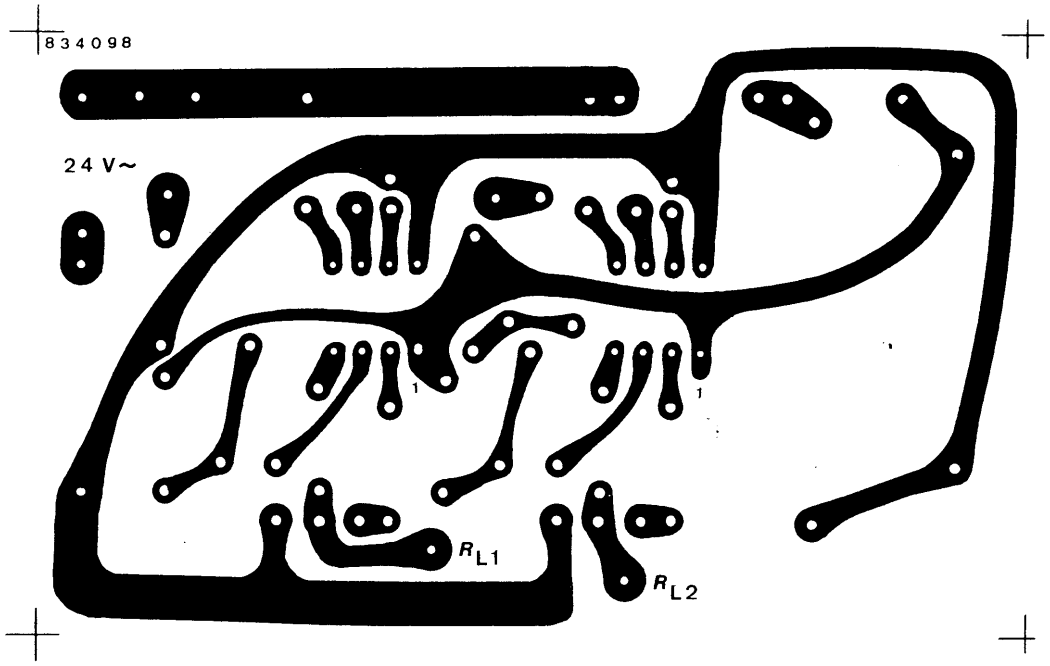


Fig. **6** Circuit board lay out

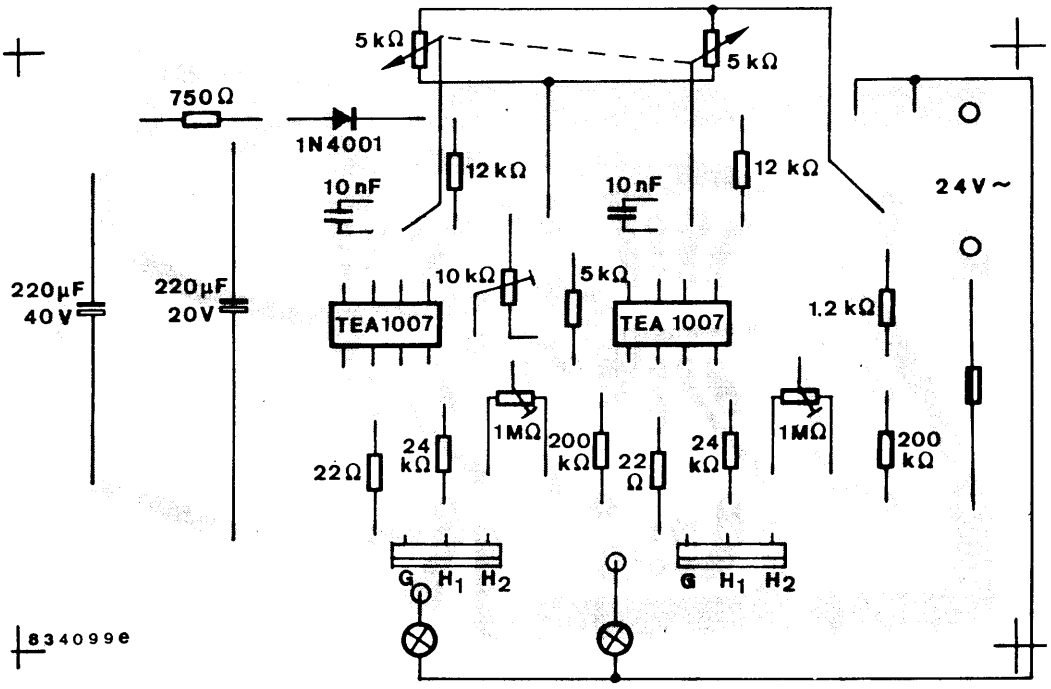
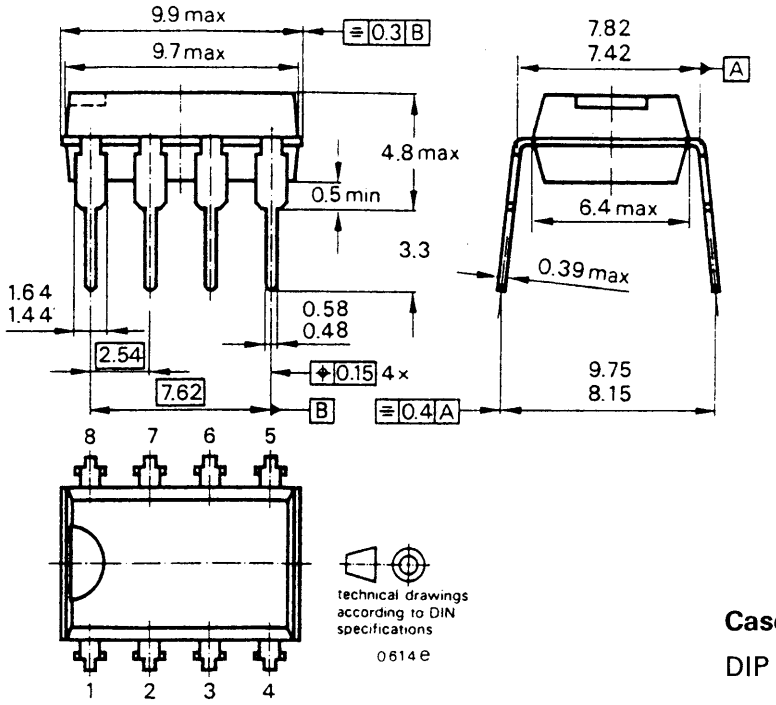


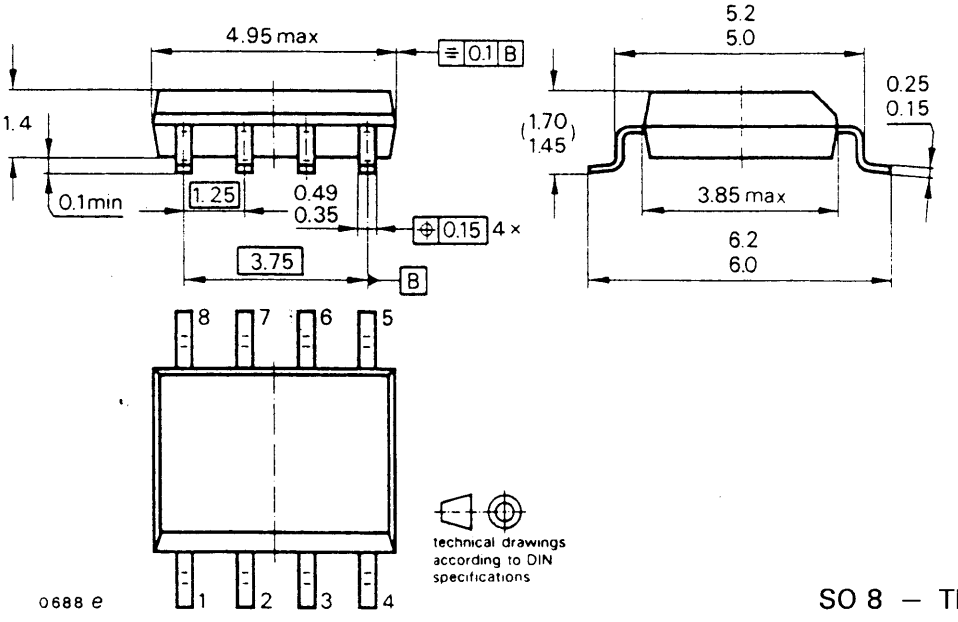
Fig. 7 Printed board with components

Dimensions in mm



Case:

DIP 8 – TEA 1007



SO 8 – TEA 1007-FP

OZONE DEPLETING SUBSTANCES POLICY STATEMENT

It is the policy of **TEMIC TELEFUNKEN microelectronic GmbH** to

1. Meet all present and future national and international statutory requirements and

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

Of particular concern is the control or elimination of releases into the atmosphere of those substances which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) will soon severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of any ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA and

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC can certify that our semiconductors are not manufactured with and do not contain ozone depleting substances.

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